BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : H01L 29/76, 29/205, 29/10 H01L 29/54, 29/64 // (H01L 29:80 H01L 29:78)	A1	(11) International Publication Number: WO 89/ 05040
		(43) International Publication Date: 1 June 1989 (01.06.89)

(21) International Application Number: PCT/US88/03850

(22) International Filing Date: 31 October 1988 (31.10.88)

(31) Priority Application Number: 123,143

(32) Priority Date: 20 November 1987 (20.11.87)

(33) Priority Country: US

(71) Applicant: BELL COMMUNICATIONS RESEARCH, INC. [US/US]; 290 West Mount Pleasant Avenue, Livingston, NJ 07039-2729 (US).

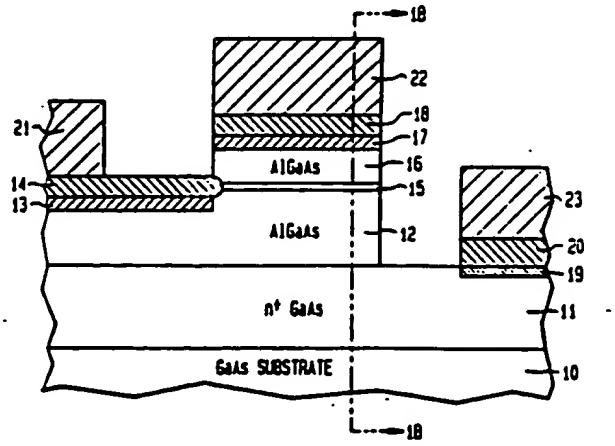
(72) Inventors: GRINBERG, Anatoly ; 401 Ridgewood Avenue #201, Minneapolis, MN 55403 (US). KASTALSKY, Alexander ; 3 Kenneth Drive, Wayside, NJ 07712 (US).

(74) Agents: WINTER, Richard, C. et al.; M.N. Meller and Associates, P.O. Box 2198, Grand Central Station, New York, NY 10163 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: QUANTUM WELL FIELD-CONTROLLED SEMICONDUCTOR TRIODE



(57) Abstract

A semiconductor device formed on a substrate (10) includes a first layer (11) of semiconductor material of a first conductivity type forming a collector (drain) region of said device; and a second layer (12) of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material disposed on the first layer (11) and forming a collector potential barrier region of the device. A third layer (15) of semiconductor material is provided composed of a relatively narrow energy bandgap material disposed on the second layer (12) and forming an emitter (source) region of the device. A fourth layer (16) of semiconductor material is further provided composed of a relatively wide energy bandgap material disposed on the third layer (15) and forming a gate region of the device. Carriers are confined in layer (15) which forms a double barrier single quantum well structure together with layers (12, 16). A Ti/AuGe/Au metallization is used for making a vertical ohmic contact to the collector region (11), a selective lateral contact to the quantum well region (15) and a Schottky contact to the gate region (16). In operation, the gate structure (16, 17, 18, 22) controls the variation of the work function for thermionic emission from the quantum well region (15) to the collector region (11) over the collector potential barrier region (12). In order to minimize a current leakage to the gate, the gate barrier in the quantum well is preferably larger than the collector barrier.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	ML	Mali
AU	Australia	GA	Gabon	MR	Mauritania
BB	Barbados	GB	United Kingdom	MW	Malawi
BE	Belgium	HU	Hungary	NL	Netherlands
BG	Bulgaria	IT	Italy	NO	Norway
BJ	Benin	JP	Japan	RO	Romania
BR	Brazil	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic			SE	Sweden
CG	Congo	KR	Republic of Korea	SN	Senegal
CH	Switzerland	LI	Liechtenstein	SU	Soviet Union
CM	Cameroon	LK	Sri Lanka	TD	Chad
DE	Germany, Federal Republic of	LU	Luxembourg	TG	Togo
DK	Denmark	MC	Monaco	US	United States of America
FI	Finland	MG	Madagascar		

QUANTUM WELL FIELD-CONTROLLED SEMICONDUCTOR TRIODE

Background of the Invention

1. Field of the Invention

The invention relates to semiconductor devices and semiconductor device fabrication, and in particular a method of forming a quantum well semiconductor device demonstrating transistor action based upon the quantum properties of electrons in a narrow quantum well, and devices made thereby.

2. Description of the Prior Art

There are a variety of different types of semiconductor devices known in the prior art. One of the more general methods of classifying these devices is in respect to the physical basis for device operation, in which there are three categories:

1. charge variation in the gate capacitor (field-effect transistors or FETs);
2. variation of a potential barrier for charge injection (e.g., bipolar, permeable base, hot electron transistors); and
3. variation of electron temperature (CHINT), as described in A. Kastalsky, J. M. Abeles, R. Bhat, W. K. Chan and M. A. Koza, *Appl. Phys. Lett.* 48, 71, (1986)

In gallium arsenide technology, a number of these different types of semiconductor devices, and semiconductor device structures have been investigated and are known in the art. GaAs MESFET devices, for example, have been quite successful in applications such as microwave and high speed digital circuits. This success of GaAs MESFET's has been due mainly to high electron velocity of GaAs and the commercial availability of semi-insulating GaAs substrates for device fabrication. Some of the drawbacks of GaAs MESFET technology are difficult circuit modeling and design, poor threshold voltage control, and the sensitivity of MESFET circuit operation to load conditions.

Bipolar technology is well known for its advantages in terms of uniform threshold, noise immunity, high speed and high current drive. A conventional bipolar transistor has an npn or pnp structure wherein emitter, based, and collector layers are made of a common semiconductor material. In this case, emitter and collector junctions are each of homojunction.

Bipolar transistors using a heterojunction as the emitter-base junction are receiving a great deal of attention and are being extensively studied these

days. The heterojunction bipolar transistor with the emitter energy gap wider than that of the base has an advantage in that, when the emitter junction is forward biased, carriers can be easily injected from the emitter to the base while carrier injection from the base to the emitter is limited due to an energy gap difference between emitter and base layers. Therefore, a current gain of the heterostructure bipolar transistor becomes higher than that of the conventional homostructure type.

In all of the semiconductor device structures of the prior art, none is based on quantum properties of the materials or structures. In other words, the basic transistor action in prior art devices is based upon and can be satisfactorily described without reference to any quantum effect. Although quantum effects may influence device performance in the prior art (for example, mobility enhancement in the 2-dimensional channel of the modulation doped FET or MODFET) or bring about useful device modification such as a tunnel emitter in the hot electron transistor, (M. Heiblum, D. C. Thomas, C. M. Knoedler and M. I. Nathan, *Appl. Phys. Lett.* 47, 1105, 1985) or in the quantum well base in the induced-based transistor (S. Luryi, *IEEE Electr. Dev. Lett.* EDL-6, 178, 1985), prior to the present invention a device has not been constructed in which the transistor action itself is based on the quantum properties of the device structure.

Summary of the Invention

Briefly, and in general terms, the present invention provides a semiconductor device implemented on a substrate including a first layer of semiconductor material of a first conductivity type forming a first active region of the device. A second layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material is disposed on the first layer and forms a second active region of the device. A third layer of semiconductor material composed of a relatively narrow energy bandgap material, is disposed on the second layer. The third layer has an energy band step such that carriers are confined in that layer, which defines a quantum well. A fourth layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material is disposed on the third layer and forms a third active region of the device. The device has contacts to the first and third layers and a Schottky barrier (gate) contact to the fourth layer. When appropriate electrical potential is provided to the active regions, the resulting structure provides a new type of transistor action that combines the properties of both bipolar and field effect transistors in a three terminal electronic device.

The novel features which are considered as characteristic for the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional

objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawing

FIG. 1a is a simplified vertical sectional view, partially diagrammatic, of a portion of a quantum well emission transistor (QWET), in accordance with a first embodiment of the present invention;

FIG. 1b shows the energy-band diagram for the section of the device shown by the sectional line in FIG. 1a;

FIG. 2 is a graph of the collector current density and transconductance versus gate voltage for a GaAs/AlGaAs-based device according to the present invention at different gate lengths;

FIG. 3 is a graph of the collector current density and transconductance versus gate voltage for an InGaAs/InAlAs band device according to the present invention at different gate lengths;

FIG. 4 is a graph showing the performance of different semiconductor devices as a function of input voltage, including the QWET according to the present invention;

FIG. 5 is a graph showing the performance of a AlGaAs/GaAs bipolar transistor (BT) in comparison with the QWET according to the present invention; and

FIG. 6 is a simplified vertical sectional view, partially diagrammatic, of a second embodiment of a QWET in accordance with the present invention.

Description of The Preferred Embodiment

FIG. 1a shows the device structure, and FIG. 1b shows the energy band diagram of the semiconductor device according to the present invention. The starting point of fabricating the semiconductor device according to the present invention is to provide a crystal wafer of gallium arsenide (GaAs) oriented in the <100> direction which forms the substrate 10. The basic method of making the semiconductor devices according to the present invention is to grow or deposit the required sequence of semiconductor crystal layers with specific doping and chemical composition on the semiconductor substrate or wafer. A plurality of distinct electronic devices may then be implemented on a major surface of the semiconductor wafer utilizing portions of such layers as active semiconductor regions. The devices may vary in structure, size, shape, composition, and function, and the use of particular layers, structures, and devices in the description hereunder are merely illustrative.

The geometry and interconnections of such devices can be defined by masking and etching according to techniques known in the art. The mesas or different

levels of the layers are formed by ion milling through a photoresist mask. The deposition of the contacts is performed by evaporation through photoresist masks. Silicon nitride is used to provide isolation between interconnections. Once such structures are defined on the wafer, the cleaving of the wafer into dice representing individual semiconductor circuits and the provision of electrical contacts to each die are well known to those skilled in the integrated circuit art.

The present description therefore focuses on the growth and deposition of the multiple layer structure on the substrate and the resulting electrical characteristics of the semiconductor device according to the present invention. There are a number of acceptable methods of crystal growth which are well known to those skilled in the semiconductor art. These include molecular beam epitaxy (MBE), and metallo-organic chemical vapor deposition (MOCVD). Either of these methods of producing the desired crystal layer structure may be selected as is appropriate for the particular device structures.

More particularly, turning to FIG. 1a, the first embodiment of the present invention provides a semiconductor device implemented on a GaAs substrate 10 including a first layer 11 of semiconductor material of a first conductivity type (n+) and forming a first active region of the device which we may designate as the "collector". A second layer 12 of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material (such as AlGaAs) is disposed on the first layer 11 and forms a second active region of the device which we may designate as the "source". A third layer 15 of semiconductor material is provided disposed on the second layer 12 and composed of a relatively narrow energy bandgap material (such as GaAs). The third layer 15 is disposed on the second layer 12 and has an energy band step such that carriers are confined in that layer. Such a layer is known as a quantum well.

A fourth layer 16 of semiconductor material of a first conductivity type is further provided composed of a relatively wide bandgap material (such as AlGaAs) disposed on the third layer 15 and forming a third active region of the device which we may designate as the "gate".

The device is provided with contacts 23 and 21 to the first and third layers respectively and Schottky barrier (gate) contact 22 to the fourth layer 16. When appropriate electrical potential is provided to the contacts and thus to the active regions, the resulting structure provides a new type of transistor action that combines the properties of both bipolar and field effect transistors in a three terminal electronic device. A more detailed analysis of different materials, structures and contact geometry will be described subsequently.

Here, we more specifically describe the device structure and the

principles of device operation in the first embodiment using the modulation doped $Al_x Ga_{1-x} As/GaAs$ heterostructure, where x is a positive number less than 1 and signifies the proportion of aluminum in the material. The results of calculation for $In_{0.47} Ga_{0.53} As$- based heterojunctions in the second embodiment will also be presented.

A key element of the structure is a thin (<100 Å) GaAs quantum well layer 15 sandwiched between $Al_x Ga_{1-x} As$ layers 12 and 16 of different Al content (x). In a preferred embodiment, the top $Al_{0.5} Ga_{0.5} As$ layer 16 is n^+ doped. The bottom insulating $Al_x Ga_{1-x} As$ layer 12 ($x \lesssim 0.4$), separates the quantum well from the n^+ GaAs layer 11, which serves as a collector region.

The contacts to the active regions are fabricated by deposition of titanium (Ti) to form layers 13, 17, and 19; followed by a deposition of a germanium gold (Ge:Au) alloy to form layers 14, 18, and 10; and finally a top contact metal (such as gold) to form layers 21, 22, and 23. The layer 14 also makes contact with the third layer 15 of semiconductor material, in addition to the second layer 12 of semiconductor material. The top gate (G) contact 22 is made as a Schottky barrier; the source (S) 21 and the collector (C) 23 contacts are low resistive ohmic contacts to the quantum well region 15 and the collector region 11, respectively.

FIG. 1b shows the band diagram of the device. We assume that when no gate voltage (V_G) is applied the quantum well has an undisturbed rectangular shape with the left wall (adjacent to the $n^+ Al_{0.5} Ga_{0.5} As$ layer) higher than the right one. A quantum well is formed from a thin layer for a first semiconductor material disposed between two layers of a second semiconductor material having an energy gap larger than the first material. Like in an ordinary energy well, carriers will be confined to the quantum well layer. Positive V_G applied relative to the source (grounded) pulls down the left wall of the quantum well and creates a quasi triangular form of potential in the quantum well. As a result of such a distortion, the energy E_1 of the ground state (counted from the energy E_c) will be lowered by $-\Delta E_1 = E_1 - E_1'$. At the same time the gate voltage increases the electron concentration n in the quantum well and raises the Fermi level relative to the ground state E_1 by the amount ΔE_F. Both ΔE_1 and ΔE_F contribute (with different sign) to the variation of the work function for thermionic emission from the quantum well to the collector giving an increment $\Delta\phi = -\Delta E_F + \Delta E_1$.

Therefore, in the case when $\Delta E_F - \Delta E_1 > 0$ the linear increase of the gate voltage will result in an exponential enhancement of the collector current density $J_C \sim exp(-\phi/kT)$. Such a variation of the output (collector) current introduces a new principle for transistor action, namely, gate controlled thermionic emission from the quantum well. Since the process of thermionic emission offers current densities as large as $\sim 10^6 A/cm^2$ (at $\phi \sim 0$) the device (which we call a Quantum Well Emission

Transistor - QWET) is expected to possess a very large current drive and a high transconductance g_m. To minimize a current leakage to the gate (due to the same process of thermionic emission), the gate side barrier in the quantum well must be larger than the collector side barrier.

For efficient operation of the QWET one needs a fast rise of the Fermi level (ΔE_F) and a slow decrease of the ground state energy ΔE_1 with V_G. This imposes certain requirements both to the material properties and to the width L of the quantum well. First, it is obvious that material with lower electron effective mass m^* provides a steeper raise of the Fermi level with increasing concentration ($\Delta E_F \sim \frac{1}{m^*}$). Secondly, to minimize the lowering of the ground state ΔE_1 one has to reduce the width of the quantum well (in the limit of infinitely narrow quantum well the effect of ground state lowering will vanish, $\Delta E_1 \to 0$). Additionally, since $\Delta E_F = \frac{C\Delta V_G}{D}$ (where $D = \frac{m^*}{\pi\hbar^2}$ is a two-dimensional density of states in the quantum well, $C = \frac{\epsilon}{d_1}$ is the capacitance per unit area, d_1 is the thickness of the n^+ AlGaAs layer), we obtain $\Delta E_F = \frac{\pi\hbar^2\epsilon\Delta V_G}{m^* d_1}$, and therefore for the given width L the use of material with lower m^* and higher dielectric constant ϵ will be beneficial for device performance. This means that InGaAs-based devices are expected to be more efficient than their GaAs/AlGaAs counterparts because of the lower m^* and higher ϵ in the former material. A natural limitation on the minimal width L of the quantum well comes from the magnitude of conduction band offset since the ground state energy in the undisturbed quantum well ($V_G = 0$) $E_1 = \frac{\pi^2\hbar^2}{2m^* L^2}$ should be lower than the barrier energy ϕ_2 at least by several kT.

Below we discuss the most important characteristics of the QWET employing a modulation doping approach. Data for both GaAs-based ($m^* = 0.07$; $\epsilon = 13$) and $In_{0.47}Ga_{0.53}As$-based ($m^* = 0.041$; $\epsilon = 13.7$) devices obtained using variational approach in the calculation of the energy $E_1(V_G)$ are presented in FIG. 2 and 3.

FIG. 2 illustrates the room temperature $j_C - V_G$ characteristics (solid lines) for GaAs-based devices materials discussed and for a set of the quantum well widths. Dashed lines are the corresponding dependences of transconductances g_m. For all cases presented the collector voltage is kept small but sufficient to neutralize a potential rise caused by the electron charge dynamically stored on the downhill slope of the collector barrier. An extreme sensitivity of the output current density j_C and the transconductance g_m to the width L is evident. As expected, j_C and g_m are small for the GaAs QW (FIG. 2) with the width $L = 80$ Å. For $L = 100$ Å we observe a clear drop of

both j_C and g_m. Much higher current densities and transconductances are obtained for $L = 60$ Å. Finally, for $L = 50$ Å and $V_G - V_{th} \approx 1V$ j_C approaches $\sim 10^5 \frac{A}{cm^2}$ with $g_m > 1\ S/mm$.

Characteristics for the InGaAs QWET, (shown in FIG. 3) reveal even much higher performance. For example, with $L = 60$ Å the maximum current density (at $V_G - V_{th} = 1.1V$) reaches $\approx 4 \times 10^5 A/cm^2$ with $g_m \approx 10\ S/mm$ (further continuation of the dependences $j_C(V_G)$ and $g_m(V_G)$ for this particular case is unphysical since at $V_G - V_{th} = 1.1V$ $\phi_2 = 0$). The comparison of an InGaAs QWET with similar characteristics ($L = 60$ Å, $V_G - V_{th} \sim 1.1V$) to the GaAs QW shows that the current density is ~300 and the transconductance is ~200 times greater for the InGaAs QWET. Thus, we come to the conclusion that the device performance crucially depends on both choice of material for the quantum well and its width. The materials with lowest carrier effective mass are preferable. The narrower the width L of the quantum well, the better the device properties that are to be expected. The limitation on L is imposed by a band discontinuity at the heterojunction forming the quantum well. The restrictions on the gate voltage swing are caused by the gate leakage due to electron transfer from the quantum well into the top n^+ AlGaAs layer occurring at high V_G. Both these features resulting from the modulation doping approach used in our calculation limit the maximum gate bias to $V_G - V_{th} \approx 1V$. Later we will describe the other device structures where these difficulties can be avoided. Now we are going to discuss the intrinsic speed of the QWET and its possible RC limitations.

As in case of the FET the intrinsic delay time τ of the QWET can be defined as $\tau = C/g_m$ where C is the gate capacitance. Using the gate insulator thickness ~300 Å and the highest values of g_m (shown in FIG. 2) we have $\tau \approx 1.2$ psec and $\tau \approx 0.15$ psec for GaAs – and InGaAs-based devices, respectively. The obtained values of τ are significantly lower than these for the equivalent parameter τ_{FET} in GaAs/AlGaAs MODFET (known as a fastest FET to date) of the same gate length L_g: $\tau_{FET} = L_g/V_{sat}$. Even for saturated velocity V_{sat} as high as 2.10^7 cm/sec and $L_g = 1\mu m$ we have $\tau_{FET} \approx 5$ psec.

However, to estimate a real delay time of our device one has to take into account RC limitations occurring mainly in its output circuit. As in the bipolar transistor we have a space-change limited (output) current flowing across the insulator to the collector, which contributes to the collector delay time $\tau_c = \frac{d_2}{V_{sat}}$, where d_2 is the thickness of insulator. Taking realistic values for $d_2 \approx 500$ Å and $V_{sat} \sim 10^7$ cm/sec we obtain $\tau_c \approx 0.5$ psec. The most essential RC limitation is expected to come from the source resistance R_S. In one embodiment, (FIG. 1) the source is connected with the active

device area through the relatively high resistive region of the quantum well which can cause a significant current restriction. A more satisfactory source contact design uses self-aligned technology for the source contact and the gate metal deposition. Contact metals (100 Å Ti) to provide a Schottky barrier to both the AlGaAs layers, and 200 Å Au:Ge alloy to make a lateral ohmic contact to the quantum well (M. Gurvitch, A. Kastalsky, S. Schwartz, D. M. Hwang, D. Butherus, S. Pearton and C. R. Gardner, *J. Appl. Phys. Lett.*, 60, 3204, 1986) are deposited by electron beam evaporation allowing a source-to-gate metal discontinuity.

However, even with such an improvement of the source contact a further reduction of the lateral channel resistance R_{ch} of the quantum well underneath the gate is still required, especially at highest achievable output currents I_c (ϕ-0) (for the device width $W \approx 100\mu m$ and the gate length $Lg \approx 1\mu m$ I_c will be in the range of 0.1 to 1A). The presence of R_{ch} results in a lateral potential drop along the channel and thereby lowers the output current in the active device area remote from the source. The latter circumstance suggests that a decrease of the gate length is beneficial for the device speed, since reduction of the gate capacitance in this case may not be accompanied by lowering of the output current. To reduce the R_{ch} it is therefore important to provide as high as possible initial ($V_G = 0$) charge density in the quantum well, which can be done either by biasing the collector or by introducing an n^+ doping into the quantum well.

The latter approach (in spite of some sacrifice in mobility) seems preferable since it allows reduction and better control of the gate threshold voltage V_T. In addition, the top AlGaAs layer can be in this case also made insulating which will result in a lower gate leakage current and a larger gate voltage swing. For the sake of estimates, let us take reasonable values for the initial channel charge density $\sim 2.10^{12}\ cm^{-2}$ and final maximum density $\sim 4\times 10^{12}\ cm^{-2}$. Having $L_g \approx 1\mu m$ we obtain $R_c \approx 0.24 \frac{\Omega}{mm}$ which for $W = 100\mu m$ and $I_c = 0.1A$ corresponds to a tolerable lateral voltage drop $\sim 0.24V$. In this case the extrinsic transconductance defined as $g_m^{ex} = \frac{g_m}{1 + g_m R_{ch}}$ for $g_m \approx 10\ S/mm$ will be equal to $g_m^{ex} \approx 3\ S/mm$. This results in the extrinsic delay time $C/g_m^{ex} \approx 0.6$ psec. Thus, even with RC limitations included our device can operate at ~1 psec delay time.

FIG. 4 is a graph showing the performance of different semiconductor devices such as a MODFET and a MESFET as a function of input voltage, the comparison with the QWET according to the present invention. FIG. 5 is a graph showing the performance of a AlGaAs/GaAs bipolar transistor (BT) in comparison with the QWET according to the present invention.

It is important to emphasize that the QWET combines the most

attractive characteristics of both the FET and the bipolar transistor. As in the bipolar transistor, our device reveals an efficient current driving ability and a high speed of operation. Unlike the bipolar transistor, however, the QWET being a unipolar device does not suffer from a charge storage limiting the speed of the BT at high current levels. As in FET, our device exhibits a high input impedance (FET insulating gate input characteristics), an extremely desirable property for logic applications.

In order to understand the relationship of device design to performance, a brief discussion of some key physical parameters of a semiconductor device is in order at this point. One of the key parameters is the delay time t, which is a measure of how fast a device is able to switch from one state (a "0" state) to another state (the "1" state). In general

$$t = \frac{c}{g_m}$$

where c is the capacity measured in farads; g_m is the transconductance, measured in 1/ohms; and t is the delay time in seconds.

The transconductance is the ratio of the change in output current to the change in input voltage. The transconductance g_m is measured in units of inverse resistivity of milliSiemens per millimeter of device width (mS/mm), where the unit "Siemens" represents the reciprocal of an ohm. A distinction is made between measured transconductance g_m and intrinsic transconductance g_{m_i}. The intrinsic transconductance is given by

$$g_{m_i} = \frac{g_m}{1 - R_s \cdot g_m}$$

R_s is the series source resistance, which may be computed from the gate voltage dependence of the drain current.

Since device performance, as measured by the delay time, is directly related to transconductance, a consideration of that parameter is important in comparing different devices. A comparison of bipolar, MESFET, and MISFET devices can be presented at this point.

The transconductance for a bipolar device is given by

$$g_m = \frac{dI_c}{dV_e}$$

while the transconductance for a MESFET is given by $g_m = \frac{dI_D}{dV_G}$. An insulated gate field effect transistor (a MISFET or IGFET) operates by creating a conducting channel in the semiconductor region beneath the gate. The conducting channel is created by virtue of a control voltage applied to the gate. In an enhancement mode device, no conductive channel exists at zero gate voltage. As a gate voltage is applied and increased beyond a threshold voltage v_T, an inversion layer is formed. The channel has a sheet conductance given by

$$g_c = \mu C_o(V_g - V_T)$$

where C_o is the capacitance per unit area of the gate electrode, and μ is the majority carrier mobility in the induced channel. More particularly,

$$C_o = E_I/T_I$$

where E_I is the dielectric constant, and T_I the thickness of the insulating layer underneath the gate.

One important relationship is the effect of scaling (change in device dimensions) on critical device parameters, such as transconductance. In a field effect transistor, as the gate length L decreases, the transconductance g_m increases according to the following relationship:

$$g_m = \frac{W}{L} \mu C_o(V_G - V_T)$$

where W is the gate width.

Because of the principles of scaling, the dominant of the speed of a field effect transistor is its gate length. The smaller the minimum gate length, the shorter the distance the electrons need to travel, and the faster the basic technology will be. The minimum transistor gate length that may be implemented commercially is determined by more than simply the capability of the most advanced semiconductor manufacturing equipment. A thorough understanding of basic transistor physics is also critically important to optimize the device design. At very small dimensions, transistors may begin to function improperly because of the physical effects of very short dimensions. These physical barriers must be understood and taken into account at each level of manufacturing. For example, the recent introduction of 0.8-micron CMOS by a number of semiconductor companies has been limited by problems associated with transistor

physics.

Another embodiment approach in fabrication of the QWET which provides improved gate characteristics is shown in FIG. 6 which represents an InGaAs-based QWET. Instead of Schottky barrier (known to be ineffective for those materials) a thin 100 - 200 Å layer of insulator such as silicon nitride (P. O'Connor, T. P. Pearsall, K. Y. Cheng, A. Y. Cho, J. C. M. Hwang and K. Alavi, *IEEE Electr. Dev. Lett.*, EDL-3, 64, 1982) or insulating InAlAs (K. Hirose, K. Ohata, T. Mizutani, T. Itoh and M. Ogawa, *Intern. Sympos GaAs and Related Compounds*, Karuizawa, 529, 1985) is deposited under the gate resulting in a reduction of the gate leakage and an increase of the gate voltage swing.

More particularly, FIG. 6 illustrates a second embodiment of the QWET semiconductor device implemented on an InGaAs substrate 30 including a first layer 31 of InGaAs semiconductor material of a first conductivity type (n+) and forming a first active region of the device which we may designate as the "collector". A second layer 32 of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material (such as InAlAs or InP) is disposed on the first layer 31 and forms a second active region of the device which we may designate as the "source". A third layer 33 of semiconductor material is provided disposed on the second layer 22 and composed of a relatively narrow energy bandgap material (such as InGaAs). The third layer 33 has an energy band step such that carriers are confined in that layer. As in the first embodiment, such a layer is a quantum well.

A fourth layer 34 of semiconductor material of a first conductivity type is further provided composed of a relatively wide bandgap material (such as InAlAs or InP) disposed on the third layer 33 and forming a third active region of the device which we may designate as the "gate". A thin layer 35 (100 to 200 Angstroms in thickness) of an insulating material, such as silicon nitride or insulating InAlAs, is disposed on the fourth layer 34 for the purposes noted above. A layer 37 of a metallic material is disposed over layer 35 to form the gate contact.

The device is provided with contacts 41 and 39 to the first and third layers respectively and a contact 40 to the gate. When appropriate electrical potential is provided to the contacts, and thus to the active regions, the resulting structure provides a new type of transistor action that has similarities and characteristics of both bipolar and field effect transistors in a single three terminal electronic device.

The contacts to the active regions are constructed by deposition of titanium (Ti) followed by a deposition of a germanium gold (Ge:Au) alloy to form composite layers 36, 37 and 38; and finally a top contact metal (such as gold) to form contacts 39, 40 and 41, respectively.

In conclusion, the present invention provides a novel transistor action based on the quantum properties of electrons confined in a quantum well. The gate modulation of charge density in the quantum well results in exponential variations of the output current of thermionic emission to the collector. The device combines the best features of both bipolar and field-effect transistors and provides a large current drive and a high speed.

While the invention has been illustrated and described as embodied in a quantum well emission semiconductor device, it is not intended to be limited to the details shown since various modifications and structural changes may be made without departing in any way from the spirit of the present invention. For example, the semiconductor materials are not limited to those shown, but may be selected from the group consisting of Group III-V, Group IV and Group II-VI semiconductors. Examples of possible combinations include InGaAsP/InP, AlGaAsSb/GaSb, AlGaAsSb/AlSb, and AlInGaAs/AlInAs.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can readily adapt it for various applications without omitting features that from the standpoint of prior art, fairly constitutes essential characteristics of the generic or specific aspects of this invention, and, therefore, such adaptations should and are intended to be comprehended within the meaning and range of equivalence of the following claims.

What is claimed is:

1. A semiconductor device implemented on a substrate comprising:

a first layer of semiconductor material of a first conductivity type disposed on said substrate and forming a first active region of said device;

a second layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap semiconductor material, disposed on said first layer and forming a second active region of the device;

a third layer composed of a relatively narrow energy bandgap semiconductor material disposed on said second layer and defining a quantum well having an energy band step such that carriers are confined in that layer; and

a fourth layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material disposed on said third layer and forming a third active region of the device.

2. A semiconductor device as defined in claim 1, wherein said first layer of semiconductor material is composed of gallium arsenide.

3. A semiconductor device as defined in claim 1, where said second layer is composed of $Al_xGa_{1-x}As$, where x is a positive number less than 1.

4. A semiconductor device as defined in claim 1, where said third layer is composed of GaAs.

5. A semiconductor device as defined in claim 1, where said second layer is composed of $Al_xGa_{1-x}As$, where x is a positive number less than 0.4.

6. A semiconductor device as defined in claim 5, where said fourth layer is composed of $Al_{0.5}Ga_{0.5}As$.

7. A semiconductor device as defined in claim 1, wherein said first layer of semiconductor material is composed of indium gallium arsenide.

8. A semiconductor device as defined in claim 7, wherein said second and said fourth layers are composed of InAlAs.

9. A semiconductor device as defined in claim 7, wherein said second and said fourth layers are composed of InP.

10. A semiconductor device as defined in claim 7, wherein said third layer is composed of InGaAs and has a thickness of less than 100 Angstroms.

11. A semiconductor device as defined in claim 7, further comprising a layer of an insulating material deposed on said fourth layer, and a layer of a metallic material disposed over said layer of insulating material.

12. A semiconductor device as defined in claim 11, wherein said insulating material is 100 to 200 Angstroms in thickness.

13. A semiconductor device as defined in claim 12 wherein said

insulating material is composed of insulating InAlAs.

14. A semiconductor device as defined in claim 1, wherein said third layer has a thickness of less than 100 Angstroms.

15. A semiconductor device as defined in claim 1, further comprising a first layer of metallic material disposed on said second layer of semiconductor material and making electrical contact with said second layer of semiconductor material for forming a first terminal of said device.

16. A semiconductor device as defined in claim 15, further comprising a second layer of metallic material disposed on said first layer of semiconductor material and making electrical contact with said first layer of semiconductor material for forming a second terminal of said device.

17. A semiconductor device as defined in claim 15, further comprising a third layer of metallic material disposed on said fourth layer of semiconductor material and making electrical contact with said fourth layer of semiconductor material for forming a third terminal of said device.

18. A semiconductor device as defined in claim 15, where said first layer of metallic material is a composite composed of a first layer of titanium, a second layer of gold/germanium making contact with said third layer of semiconductor material, and a third layer of gold.

19. A semiconductor device as defined in claim 16, where said second layer of metallic material is a composite composed of a first layer of titanium, a second layer of gold/germanium, and a third layer of gold.

20. A semiconductor device as defined in claim 17, where said third layer of metallic material is a composite composed of a first layer of titanium, a second layer of gold/germanium, and a third layer of gold.

21. A device as defined in claim 1, wherein said first layer forms the collector region during transistor action of said device.

22. A device as defined in claim 1, wherein said second layer forms the source region during transistor action of said device.

23. A device as defined in claim 1, wherein said fourth layer forms the gate region during transistor action of said device.

24. A method for making a semiconductor device implemented on a substrate comprising:

depositing a first layer of semiconductor material of a first conductivity type on said substrate to form a first active region of said device;

depositing a second layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap semiconductor material

on said first layer to form a second active region of the device;

depositing a third layer composed of a relatively narrow energy bandgap semiconductor material on said second layer, said third layer having an energy band step such that carriers are confined in that layer and such layer forming a quantum well;

depositing a fourth layer of semiconductor material of a first conductivity type composed of a relatively wide energy bandgap material on said third layer to form a third active region of the device; and

providing electrical contacts to said first, third and fourth layers for forming a three terminal electron device.

FIG. 1B

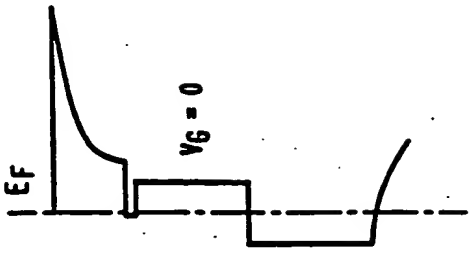

E_F
$V_G = 0$

FIG. 1A

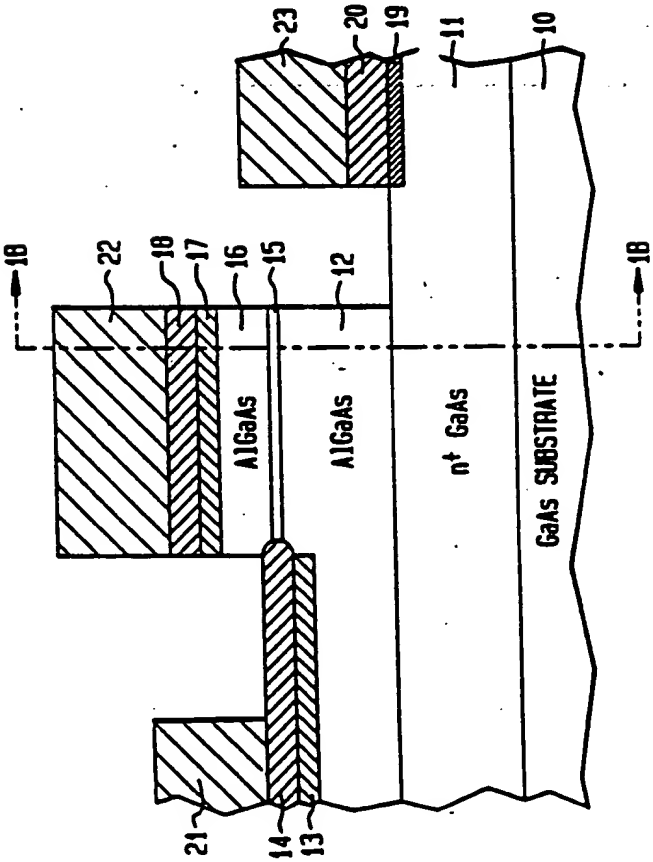

23
20
19
11
10
18
22
18
17
16
15
12
18
AlGaAs
AlGaAs
n+ GaAs
GaAs SUBSTRATE
21
14
13

FIG. 2

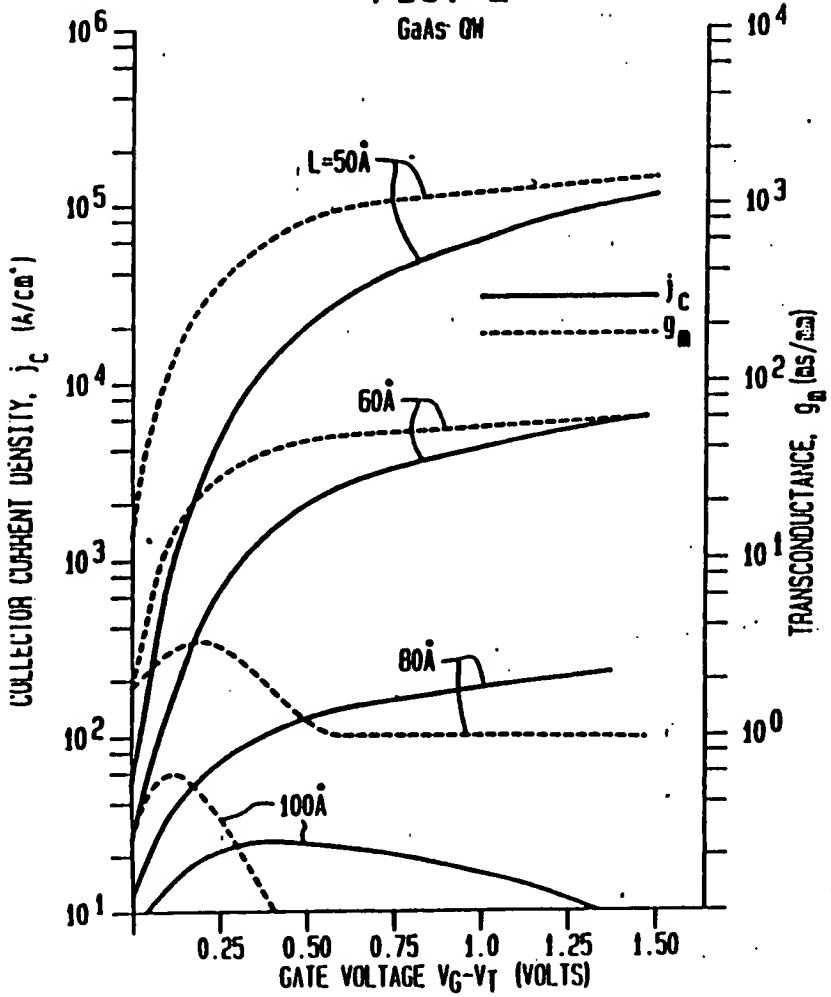

GaAs QW
L=50Å
60Å
80Å
100Å
j_c
g_m
COLLECTOR CURRENT DENSITY, j_c (A/cm²)
TRANSCONDUCTANCE, g_m (mS/mm)
GATE VOLTAGE V_G-V_T (VOLTS)
10^6
10^5
10^4
10^3
10^2
10^1
10^4
10^3
10^2
10^1
10^0
0.25
0.50
0.75
1.0
1.25
1.50

FIG. 3

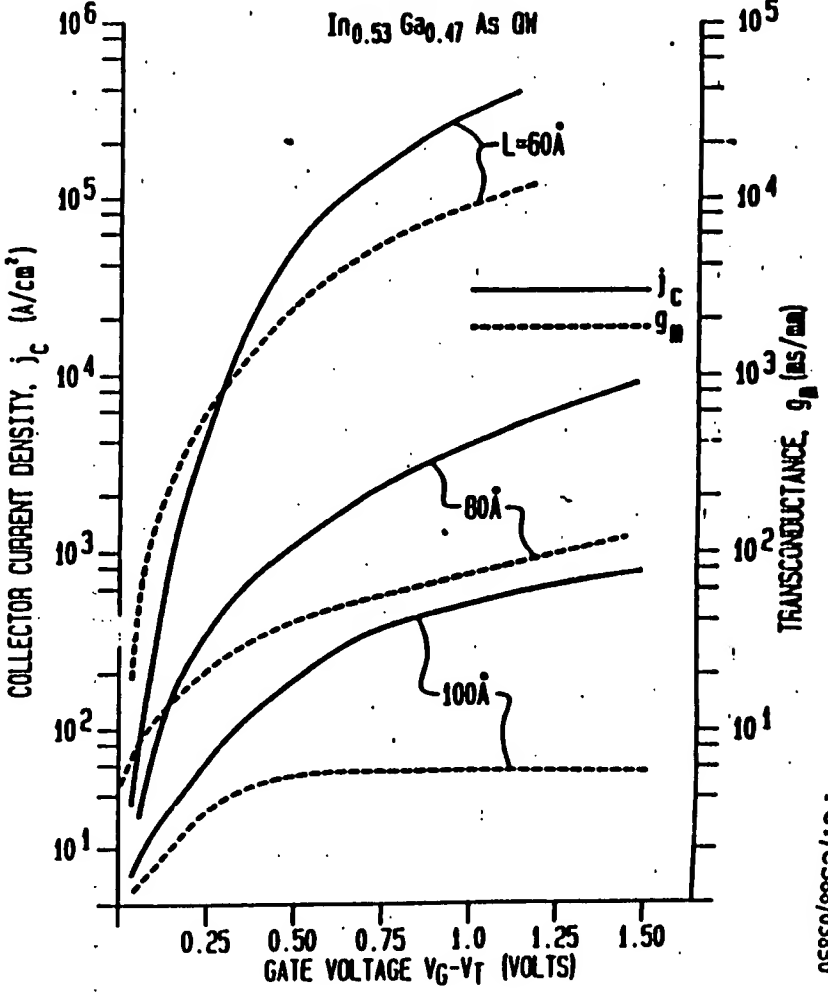

$In_{0.53}Ga_{0.47}As$ QW
L=60Å
80Å
100Å
j_c
g_m
COLLECTOR CURRENT DENSITY, j_c (A/cm²)
TRANSCONDUCTANCE, g_m (mS/mm)
GATE VOLTAGE V_G-V_T (VOLTS)
10^6
10^5
10^4
10^3
10^2
10^1
10^5
10^4
10^3
10^2
10^1
0.25
0.50
0.75
1.0
1.25
1.50

FIG. 4

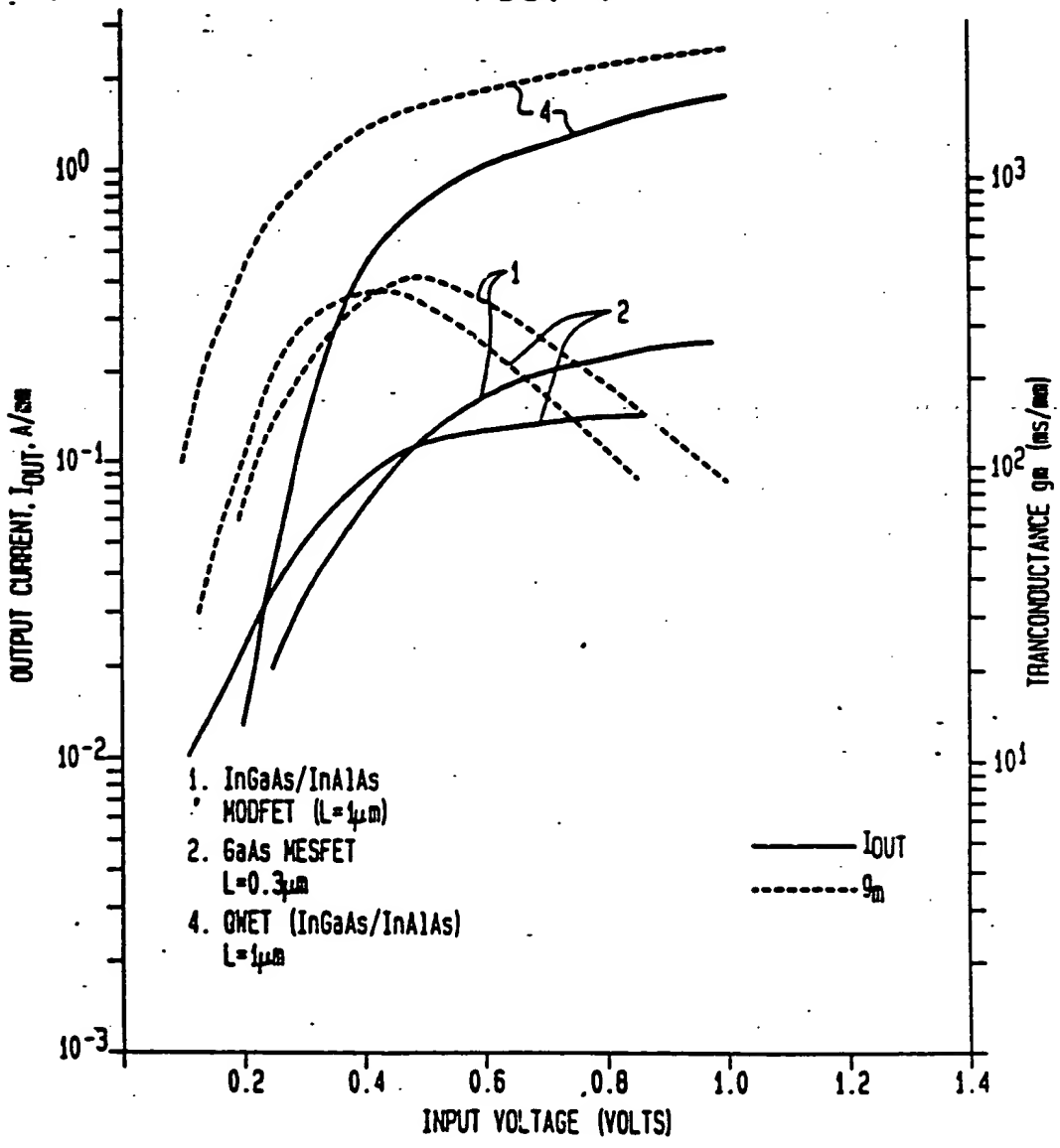
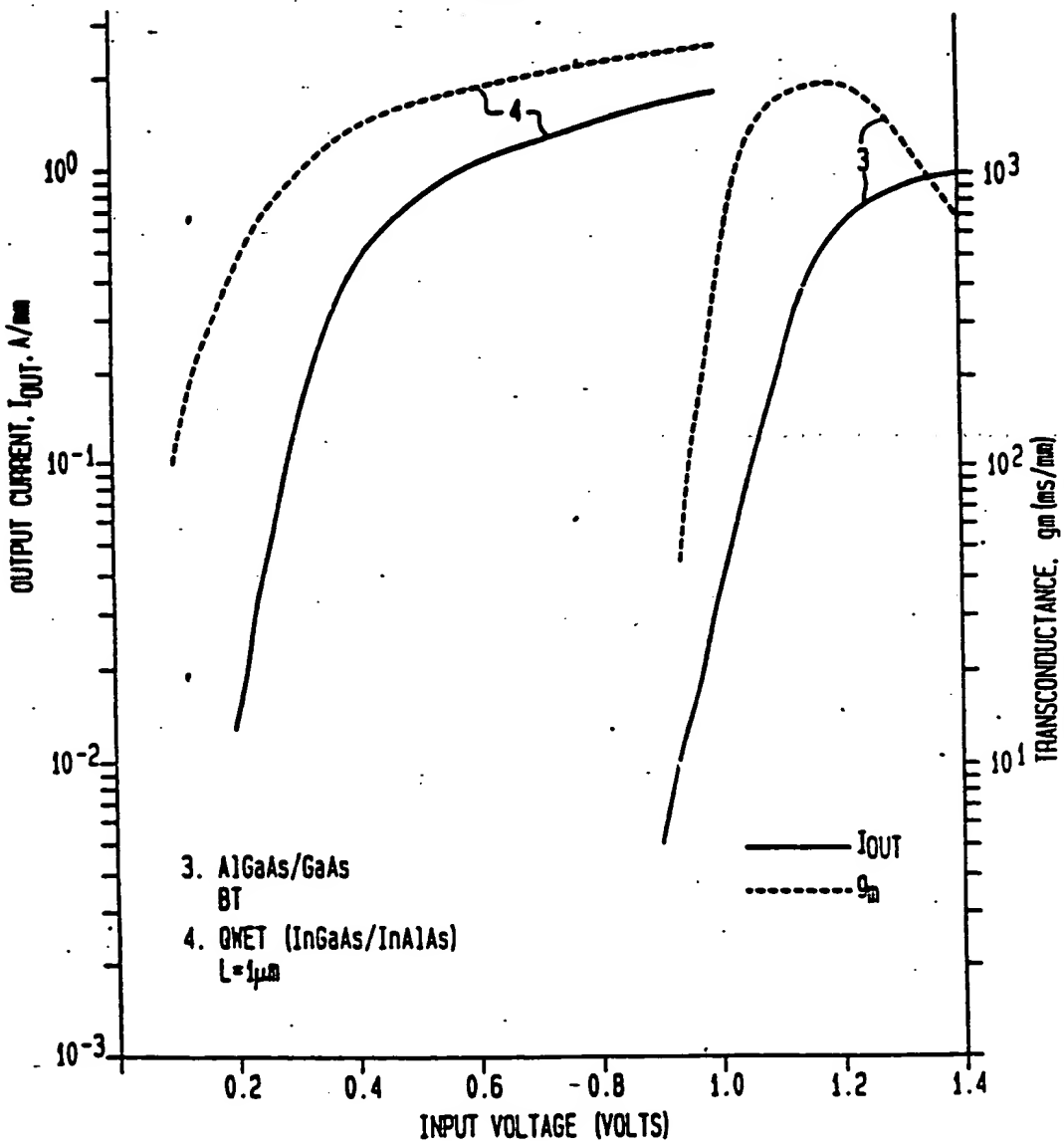

OUTPUT CURRENT, I_{OUT}, A/mm
TRANCONDUCTANCE g_m (ms/mm)
INPUT VOLTAGE (VOLTS)
10^0
10^{-1}
10^{-2}
10^{-3}
10^3
10^2
10^1
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1
2
4
1. InGaAs/InAlAs MODFET (L=1μm)
2. GaAs MESFET L=0.3μm
4. QWET (InGaAs/InAlAs) L=1μm
I_{OUT}
g_m

FIG. 5


OUTPUT CURRENT, I_{OUT}, A/mm
10^0
10^{-1}
10^{-2}
10^{-3}
TRANSCONDUCTANCE, g_m (ms/mm)
10^3
10^2
10^1
4
3
0.2
0.4
0.6
-0.8
1.0
1.2
1.4
INPUT VOLTAGE (VOLTS)
3. AlGaAs/GaAs
BT
4. QWET (InGaAs/InAlAs)
L=1μm
I_{OUT}
g_m

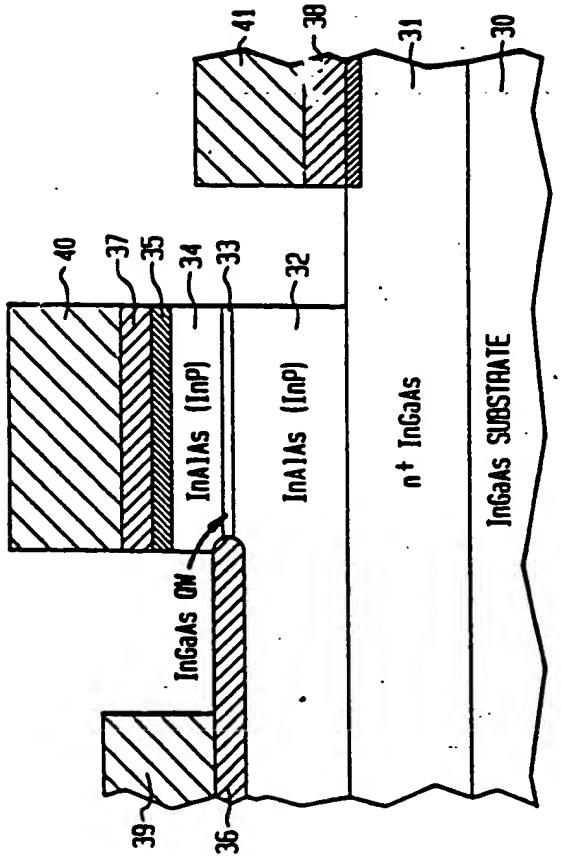

41
38
31
30
40
37
35
34
33
32
InAlAs (InP)
InAlAs (InP)
n+ InGaAs
InGaAs SUBSTRATE
InGaAs ON
39
36

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 88/03850

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 29/76; 29/205; 29/10; 29/54; 29/64;//H 01 L 29/80; H 01 L 29/78

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System [8]	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [9]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	Patent Abstracts of Japan, vol. 10, no. 259, (E-434)(2315), 4th September 1986 & JP, A, 6184871 (HITACHI LTD) 30 April 1986, see abstract; figures	1-5,15-17, 21-24
A	IEEE Electron Device Letters, vol. EDL-6, no. 7, July 1985 (New York, US) K. Hikosaka et al.: "A microwave power double-heterojunction high electron mobility transistor" pages 341-343, see pages 341,342, paragraph II	1,3-5,14, 15,17,22-24
X	EP, A, 0091831 (SAKAKI) 19 October 1983, see page 3, lines 7-21; figure 1	1-4,15-17, 22-24
A	IEEE Transactions on Electron Devices, vol. ED-31, no. 6, June 1984 (New York, US) S. Luryi et al.: "Charge injection transistor based on real-space hot-electron transfer", pages 832-839, see pages 833-834, paragraph II;	1-5,7,8, 10,15-17, 21-24

./.

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of the International Search Report
15th March 1989	07 APR 1989
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	page 838, right-hand column; figure 2	
A	IBM Technical Disclosure Bulletin, vol. 26, no. 10A, March 1984 (New York, US) W.P. Dumke: "Accelerated electron transistor", pages 5275-5277 see figures 1-3	1-6,15,16, 21,22,24
A	Proceedings IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits" 29,30,31 July 1985, Ithaca, N.Y. IEEE, New York (US) K. Seo et al.: "Properties of a $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ single quantum well MISFET", pages 102-110, see pages 102,103,105; figure 1	1,8,10,11, 13,15,17, 22-24
A	EP, A, 0050064 (THOMSON-CSF) 21 April 1982, see page 4, lines 12-23; page 5, lines 20-28; figure 5	1,8-10, 15,17,22-24
A	Inst. Phys. Conf. Ser. No. 79: Chapter 10, Int. Symp. GaAs and Related Compounds, Karuizawa, JP, 1985 Adam Hilger Ltd K. Hirose et al.: "700 mS/mm 2DEGFETs fabricated from high mobility MBE-grown n-AlInAs/GaInAs heterostructures" pages 529-534, see figure 2 (cited in the application)	1,8,10-13, 15,17,22-24

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8803850 SA 25726

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 05/04/89
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0091831	19-10-83	JP-A- 58178572	19-10-83
		US-A- 4688061	18-08-87
EP-A- 0050064	21-04-82	FR-A,B 2492167	16-04-82
		JP-A- 57095672	14-06-82
		CA-A- 1182930	19-02-85